| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| | | | |

| | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | | | | | | | | | | | | | | |
| REV STATUS OF SHEETS | | | | REV | | | | | | | | | | | | | | | | |
| | | | | SHEET | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

**STANDARDIZED MILITARY DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

**AMSC N/A**

PREPARED BY
Joseph A. Kerby

CHECKED BY
Thanh V. Nguyen

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
94-06-23

REVISION LEVEL

**DEFENSE ELECTRONIC SUPPLY CENTER**
**DAYTON, OHIO 45444**

MICROCIRCUITS, DIGITAL, FAST CMOS, NONINVERTING OCTAL REGISTERED TRANSCEIVER WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS AND LIMITED OUTPUT VOLTAGE SWING, MONOLITHIC SILICON

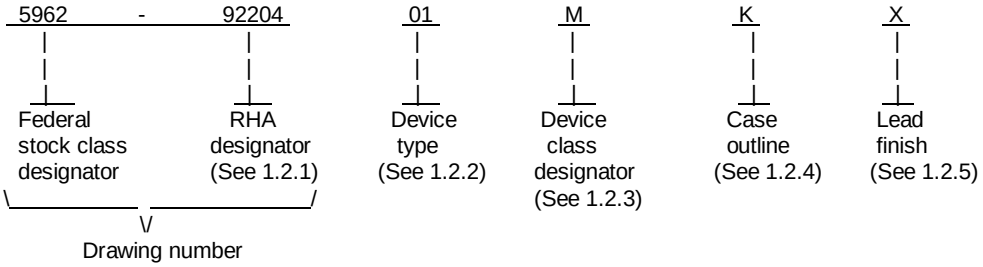
| SIZE | CAGE CODE | |
|---|---|---|
| **A** | 67268 | **5962-92204** |

SHEET 1 OF 20

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:




1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 29FCT52AT | Noninverting octal registered transceiver with three-state outputs, TTL compatible inputs and limited output voltage swing. |
| 02 | 29FCT52BT | Noninverting octal registered transceiver with three-state outputs, TTL compatible inputs and limited output voltage swing. |
| 03 | 29FCT52CT | Noninverting octal registered transceiver with three-state outputs, TTL compatible inputs and limited output voltage swing. |

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883 |
| Q or V | Certification and qualification to MIL-I-38535 |

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| K | GDFP2-F24 or CDFP3-F24 | 24 | Flat package |
| L | GDIP3-T24 or CDIP4-T24 | 24 | Dual-in-line package |
| 3 | CQCC1-N28 | 28 | Leadless-chip-carrier package |

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/ 2/ 3/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | -0.5 V dc to +7.0 V dc |
| DC input voltage range ($V_{IN}$) | -0.5 V dc to $V_{CC}$ + 0.5 V dc 4/ |
| DC output voltage range ($V_{OUT}$) | -0.5 V dc to $V_{CC}$ + 0.5 V dc 4/ |
| DC input clamp current ($I_{IK}$) ($V_{IN}$ = -0.5 V) | -20 mA |
| DC output clamp current ($I_{OK}$) ($V_{OUT}$ = -0.5 V and +7.0 V) | ±20 mA |
| DC output source current ($I_{OH}$) per output | -30 mA |
| DC output sink current ($I_{OL}$) per output | +70 mA |
| DC $V_{CC}$ current ($I_{CC}$) | ±260 mA |
| DC ground current ($I_{GND}$) | ±550 mA |
| Storage temperature range ($T_{STG}$) | -65° C to +150° C |
| Case temperature under bias ($T_{BIAS}$) | -65° C to +135° C |
| Maximum power dissipation ($P_D$) | 500 mW |
| Lead temperature (soldering, 10 seconds) | +300° C |
| Thermal resistance, junction-to-case ($\Theta_{JC}$) | See MIL-STD-1835 |
| Junction temperature ($T_J$) | +175° C |

1.4 Recommended operating conditions. 2/ 3/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | +4.5 V dc to +5.5 V dc |
| Input voltage range ($V_{IN}$) | +0.0 V dc to $V_{CC}$ |
| Output voltage range ($V_{OUT}$) | +0.0 V dc to $V_{CC}$ |
| Maximum low level input voltage ($V_{IL}$) | 0.8 V |
| Minimum high level input voltage ($V_{IH}$) | 2.0 V |
| Case operating temperature range ($T_C$) | -55° C to +125° C |
| Maximum input rise and fall rate ($\Delta t/\Delta V$): (from $V_{IN}$ = 0.3 V to 2.7 V, 2.7 V to 0.3 V) | 5 ns/V |
| Maximum high level output current ($I_{OH}$) | -12 mA |
| Maximum low level output current ($I_{OL}$) | 48 mA |

1.5 Digital logic testing for device classes Q and V.

| | |
|---|---|
| Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) | XX percent 5/ |

---

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified $V_{CC}$ range and case temperature range of -55° C to +125° C.

4/ For $V_{CC} \geq 6.5$ V, the upper limit on the range is limited to 7.0 V.

5/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforms shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range. Test conditions for these specified characteristics and limits are as specified in table I.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 37 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

TABLE I. Electrical performance characteristics.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified | | Device type | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Min | Max | |
| High level output voltage 3006 | $V_{OH1}$ 4/ | For all inputs affecting output under test $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -300\ \mu A$ | | All | 4.5 V | 1, 2, 3 | 3 | $V_{CC}$ - 0.5 | V |
| | $V_{OH2}$ | For all inputs affecting output under test $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -12\ mA$ | | All | 4.5 V | 1, 2, 3 | 2.4 | $V_{CC}$ - 0.5 | |
| Low level output voltage 3007 | $V_{OL1}$ 4/ | For all inputs affecting output under test $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 300\ \mu A$ | | All | 4.5 V | 1, 2, 3 | | 0.2 | |
| | $V_{OL2}$ | For all inputs affecting output under test $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 48\ mA$ | | All | 4.5 V | 1, 2, 3 | | 0.55 | |
| Three-state output leakage current high 3021 | $I_{OZH}$ 5/ 6/ | $\overline{OEA} = \overline{OEB} = V_{IH}$ or $V_{IL}$ $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND | $V_{OUT} = V_{CC}$ | All | ,5.5 V | 1, 2 | | 1.0 | $\mu A$ |
| | | | | | | 3 | | 10.0 | |
| Three-state output leakage current low 3021 | $I_{OZL}$ 5/ 6/ | $\overline{OEA} = \overline{OEB} = V_{IH}$ or $V_{IL}$ $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND | $V_{OUT} = GND$ | All | ,5.5 V | 1, 2 | | -1.0 | |
| | | | | | | 3 | | -10.0 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics.- Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified | | Device type | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Min | Max | |
| Negative input clamp voltage 3022 | $V_{IC}$- | For input under test, $I_{IN}$ = -18 mA | | All | 4.5 V | 1, 2, 3 | | -1.2 | V |
| Input current high 3010 | $I_{IH}$ | For input under test $V_{IN} = V_{CC}$ For all other inputs $V_{IN} = V_{CC}$ or GND | Control inputs | All | 5.5 V | 1, 2 | | 1.0 | µA |
| | | | | | | 3 | | 5.0 | |
| | | | I/O pins | | | 1, 2 | | 2.0 | |
| | | | | | | 3 | | 15.0 | |
| Input current low 3010 | $I_{IL}$ | For input under test $V_{IN}$ = GND For all other inputs $V_{IN} = V_{CC}$ or GND | Control inputs | All | 5.5 V | 1, 2 | | -1.0 | µA |
| | | | | | | 3 | | -5.0 | |
| | | | I/O pins | | | 1, 2 | | -2.0 | |
| | | | | | | 3 | | -15.0 | |
| Input capacitance 3012 | $C_{IN}$ 7/ | See 4.4.1b $T_C$ = +25°C | | All | GND | 4 | | 10 | pF |
| Input/output capacitance 3012 | $C_{I/O}$ 7/ | See 4.4.1b $T_C$ = +25°C | | All | GND | 4 | | 12 | pF |
| Short circuit output current 3011 | $I_{OS}$ 8/ | For all inputs $V_{IN} = V_{CC}$ or GND $V_{OUT}$ = GND | | All | 5.5 V | 1,2 ,3 | -60 | -225 | mA |
| Dynamic Power supply current | $I_{CCD}$ 4/ 9/ | Outputs open | | All | 5.5 V | 4, 5, 6 | | 0.25 | mA/ Mhz.Bit |
| Quiescent supply current delta, TTL input levels 3005 | $\Delta I_{CC}$ 10/ | For input under test $V_{IN} = V_{CC}$ - 2.1 V For all other inputs $V_{IN} = V_{CC}$ or GND | | All | .5.5 V | 1, 2, 3 | | .2.0 | mA |
| Power down disable | $I_{OFF}$ 11/ | For output under test $V_{OUT}$ = 4.5 V For other pins at 0.0 V | | All | 0.0 V | 1, 2 | | 1.0 | µA |
| | | | | | | 3 | | 5.0 | |
| Quiescent supply current, output high 3005 | $I_{CCH}$ | $\overline{OEA} = \overline{OEB}$ = GND For all other inputs $V_{IN} = V_{CC}$ or GND | | All | 5.5 V | 1, 2, 3 | | 1.5 | mA |

See footnotes at end of table.

TABLE I. Electrical performance characteristics.- Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified | | Device type | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Min | Max | |
| Quiescent supply current, output low 3005 | $I_{CCL}$ | $\overline{OEA} = \overline{OEB} = GND$<br>For all other inputs<br>$V_{IN} = V_{CC}$ or GND | | All | 5.5 V | 1, 2, 3 | | 1.5 | mA |
| Quiescent supply current, output three-state 3005 | $I_{CCZ}$ | $\overline{OEA} = \overline{OEB} = V_{CC}$<br>For all other inputs<br>$V_{IN} = V_{CC}$ or GND | | All | 5.5 V | 1, 2, 3 | | 1.5 | mA |
| Total supply current | $I_{CCT}$ | Outputs open<br>OEA = OEB = GND<br>$f_{CP}$ = 10 MHz<br>50% duty cycle<br>One bit toggling at<br>$f_i$ = 5 MHz<br>50% duty cycle<br>For nonswitching inputs,<br>$V_{IN} = V_{CC}$ or GND | For switching inputs<br>$V_{IN} = V_{CC}$ or GND | All | 5.5 V | 4, 5, 6 | | 4.0 | mA |
| | | | For switching inputs<br>$V_{IN}$ = 3.4 V or GND | | | 4, 5, 6 | | 6.0 | |
| | | Outputs open<br>OEA = OEB = GND<br>$f_{CP}$ = 10 MHz<br>50% duty cycle<br>Eight bits toggling<br>$f_i$ = 5 MHz<br>50% duty cycle<br>For nonswitching inputs,<br>$V_{IN} = V_{CC}$ or GND | For switching inputs<br>$V_{IN} = V_{CC}$ or GND | | | 4, 5, 6 | | 7.8 | |
| | | | For switching inputs<br>$V_{IN}$ = 3.4 V or GND | | | 4, 5, 6 | | 16.8 | |
| Low level ground bounce noise | $V_{OLP}$ 7/ 13/ | $V_{IH}$ = 3.0 V<br>$V_{IL}$ = 0.0 V<br>$T_A = +25°C$<br>See figure 4 | | All | 5.0 V | 4 | | | mV |
| Low level ground bounce noise | $V_{OLV}$ 7/ 13/ | | | All | 5.0 V | 4 | | | mV |
| High level $V_{CC}$ bounce noise | $V_{OHP}$ 7/ 13/ | | | All | 5.0 V | 4 | | | mV |
| High level $V_{CC}$ bounce noise | $V_{OHV}$ 7/ 13/ | | | All | 5.0 V | 4 | | | mV |

See footnotes at end of table.

TABLE I. Electrical performance characteristics.- Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified | Device type | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Functional test 3014 | 14/ | $V_{IL} = 0.8\ V$; $V_{IH} = 2.0\ V$<br>Verify output $V_O$<br>See 4.4.1d | All | 4.5 V | 7, 8 | L | H | |
| | | $V_{IL} = 0.8\ V$; $V_{IH} = 2.0\ V$<br>Verify output $V_O$<br>See 4.4.1d | All | 5.5 V | 7, 8 | L | H | |
| Propagation delay time, CPA to An CPB to Bn | $t_{PHL}$, $t_{PLH}$ | $C_L = 50$ pF minimum,<br>$R_L = 500\ \Omega$,<br>See figure 5 | 01 | 4.5 V | 9, 10, 11 | 2.0 | 11.0 | ns |
| | | | 02 | | 9, 10, 11 | 2.0 | 8.0 | |
| 3003 | 15/ | | 03 | | 9, 10, 11 | 2.0 | 7.3 | |
| Propagation delay time, output enable, OEA to An, OEB to Bn 3003 | $t_{PZH}$, $t_{PZL}$ | $C_L = 50$ pF minimum,<br>$R_L = 500\ \Omega$,<br>See figure 5 | 01 | 4.5 V | 9, 10, 11 | 1.5 | 13.0 | |
| | | | 02 | | 9, 10, 11 | 1.5 | 8.5 | |
| | 15/ | | 03 | | 9, 10, 11 | 1.5 | 8.0 | |
| Propagation delay time, output disable, OEA to An, OEB to Bn 3003 | $t_{PHZ}$, $t_{PLZ}$ | $C_L = 50$ pF minimum,<br>$R_L = 500\ \Omega$,<br>See figure 5 | 01 | 4.5 V | 9, 10, 11 | 1.5 | 10.0 | ns |
| | | | 02 | | 9, 10, 11 | 1.5 | 8.0 | |
| | 15/ | | 03 | | 9, 10, 11 | 1.5 | 7.5 | |
| Set_up time, data high or low, An to CPA, Bn to CPB | $t_{S1}$ | $C_L = 50$ pF minimum,<br>$R_L = 500\ \Omega$,<br>See figure 5 | 01 | 4.5 V | 9, 10, 11 | 2.5 | | ns |
| | 15/ | | 02 | | 9, 10, 11 | 2.5 | | |
| | | | 03 | | 9, 10, 11 | 2.5 | | |
| Set_up time, data high or low, CEA to CPA, CEB to CPB | $t_{S1}$ | $C_L = 50$ pF minimum,<br>$R_L = 500\ \Omega$,<br>See figure 5 | 01 | 4.5 V | 9, 10, 11 | 3.0 | | ns |
| | 15/ | | 02 | | 9, 10, 11 | 3.0 | | |
| | | | 03 | | 9, 10, 11 | 3.0 | | |
| Hold time, data high or low, An to CPA, Bn to CPB | $t_{h1}$ | $C_L = 50$ pF minimum,<br>$R_L = 500\ \Omega$,<br>See figure 5 | 01 | 4.5 V | 9, 10, 11 | 2.0 | | ns |
| | 15/ | | 02 | | 9, 10, 11 | 1.5 | | |
| | | | 03 | | 9, 10, 11 | 1.5 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics.- Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified | Device type | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Hold time, data high or low, CEA to CPA, CEB to CPB | $t_{h2}$ 15/ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, See figure 5 | 01 | 4.5 V | 9, 10, 11 | 2.0 | | ns |
| | | | 02 | | 9, 10, 11 | 2.0 | | |
| | | | 03 | | 9, 10, 11 | 2.0 | | |
| Clock pulse width, high or low | $t_w$ 15/ | $C_L$ = 50 pF minimum, $R_L$ = 500 Ω, See figure 5 | 01 | 4.5 V | 9, 10, 11 | 3.0 | | ns |
| | | | 02 | | 9, 10, 11 | 3.0 | | |
| | | | 03 | | 9, 10, 11 | 3.0 | | |

1/ For tests not listed in the referenced MIL-STD-883 (e.g. $\Delta I_{CC}$), utilize the general test procedure of 883 under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all $I_{CC}$ and $\Delta I_{CC}$ tests, the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I at $4.5\ V \le V_{CC} \le 5.5\ V$.

4/ This parameter is guaranteed, if not tested, to the limits specified in table I.

5/ Three-state output conditions are required.

6/ This test may be performed using $V_{IH}$ = 3.0 V. When $V_{IH}$ = 3.0 V is used, the test is guaranteed for $V_{IH}$ = 2.0 V. This test is guaranteed by the $I_{IL}$ and $I_{IH}$ tests.

7/ This test is required only for group A testing; see 4.4.1 herein.

8/ Not more than one output should be shorted at a time. The duration of the short circuit test should not exceed one second.

9/ $I_{CCD}$ may be verified by the following equation:

$$I_{CCD} = \frac{I_{CCT} - I_{CC} - D_H N_T \Delta I_{CC}}{f_{CP}/2 + f_i N_i}$$

where $I_{CCT}$, $I_{CC}$ ($I_{CCL}$ or $I_{CCH}$ in table I), and $\Delta I_{CC}$ shall be the measured values of these parameters, for the device under test, when tested as described in table I, herein. The values for $D_H$, $N_T$, $f_{CP}$, $f_i$, $N_i$ shall be as listed in the test conditions column for $I_{CCT}$ in table I, herein.

10/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1\ V$ (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 2.0 mA; and the preferred method and limits are guaranteed.

11/ For $I_{OFF}$ testing, test each output.

TABLE I. Electrical performance characteristics - Continued.

12/ $I_{CCT}$ is calculated as follows:
$I_{CCT} = I_{CC} + D_H N_T \Delta I_{CC} + I_{CCD}(f_{CP}/2 + f_i N_i)$

where

$I_{CC}$ = Quiescent supply current (any $I_{CCL}$ or $I_{CCH}$)
$D_H$ = Duty cycle for TTL inputs at 3.4 V
$N_T$ = Number of TTL inputs at 3.4 V
$\Delta I_{CC}$ = Quiescent supply current delta, TTL inputs at 3.4 V
$I_{CCD}$ = Dynamic power supply current caused by an input transition pair (HLH or LHL)
$f_{CP}$ = Clock frequency for registered devices ($f_{CP}$ = 0 for nonregistered devices)
$f_i$ = Input frequency
$N_i$ = Number of inputs at $f_i$

13/ This test is for qualification only. Ground and $V_{CC}$ bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500 Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 4). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than .25 inches. Decoupling capacitors shall be placed in parallel from $V_{CC}$ to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and $V_{CC}$ bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal $V_{OH}$ level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at $V_{OH}$ as all other outputs possible are switched from $V_{OH}$ to $V_{OL}$. $V_{OHV}$ and $V_{OHP}$ are then measured from the nominal $V_{OH}$ level to the largest negative and positive peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from $V_{OL}$ to $V_{OH}$.

The device inputs shall be conditioned such that all outputs are at a low nominal $V_{OL}$ level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at $V_{OL}$ as all other outputs possible are switched from $V_{OL}$ to $V_{OH}$. $V_{OLP}$ and $V_{OLV}$ are then measured from the nominal $V_{OL}$ level to the largest positive and negative peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from $V_{OH}$ to $V_{OL}$.

The $V_{CC}$ and ground bounce tests were not completed at the date of this drawing. Limits for these parameters shall be added by revision no more than 90 days from the date of this drawing.

14/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth tables and other logic patterns used for fault detection. The test vectors used to verify the truth tables shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth tables in figure 2, herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. H ≥ 1.5 V, L < 1.5 V.

15/ AC limits at $V_{CC}$ = 5.5 V are equal to the limits at $V_{CC}$ = 4.5 V and guaranteed by testing at $V_{CC}$ = 4.5 V. Minimum propagation delay time limits for $V_{CC}$ = 4.5 V and 5.5 V are guaranteed if not tested to the limits specified in table I, herein. For ac tests, all paths must be tested.

| Device types | 01, 02, 03 | | | | |
|---|---|---|---|---|---|
| Case outlines | L and K | 3 | Case outlines | L and K | 3 |
| Terminal number | Terminal symbol | | Terminal number | Terminal symbol | |
| 1 | B7 | NC | 15 | $\overline{OEA}$ | NC |
| 2 | B6 | B7 | 16 | A0 | $\overline{CEB}$ |
| 3 | B5 | B6 | 17 | A1 | CPB |
| 4 | B4 | B5 | 18 | A2 | $\overline{OEA}$ |
| 5 | B3 | B4 | 19 | A3 | A0 |
| 6 | B2 | B3 | 20 | A4 | A1 |
| 7 | B1 | B2 | 21 | A5 | A2 |
| 8 | B0 | NC | 22 | A6 | NC |
| 9 | $\overline{OEB}$ | B1 | 23 | A7 | A3 |
| 10 | CPA | B0 | 24 | $V_{CC}$ | A4 |
| 11 | $\overline{CEA}$ | $\overline{OEB}$ | 25 | --- | A5 |
| 12 | GND | CPA | 26 | --- | A6 |
| 13 | $\overline{CEB}$ | $\overline{CEA}$ | 27 | --- | A7 |
| 14 | CPB | GND | 28 | --- | $V_{CC}$ |

| Pin descriptions | |
|---|---|
| Terminal symbol | Description |
| CPA (input) | Clock for A register. When $\overline{CEA}$ is low, data is entered into the A register on the low-to-high transition of the CPA signal |
| CPB (input) | Clock for B register. When $\overline{CEB}$ is low, data is entered into the B register on the low-to-high transition of the CPB signal |
| $\overline{CEA}$ (input) | Clock enable for the A register. When $\overline{CEA}$ is low, data is entered into the A register on the low-to-high transition of the CPA signal. When $\overline{CEA}$ is high, the A register holds its contents, regardless of CPA signal transition |
| $\overline{CEB}$ (input) | Clock enable for the B register. When $\overline{CEB}$ is low, data is entered into the B register on the low-to-high transition of the CPB signal. When $\overline{CEB}$ is high, the B register holds its contents, regardless of CPB signal transition |
| $\overline{OEA}$ (input) | Output enable for the B register. When $\overline{OEA}$ is low, the B register outputs are enabled onto the A0-A7 lines. When $\overline{OEA}$ is high, the A0-A7 outputs are in the high-impedance state. |
| $\overline{OEB}$ (input) | Output enable for the A register. When $\overline{OEB}$ is low, the A register outputs are enabled onto the B0-B7 lines. When $\overline{OEB}$ is high, the B0-B7 outputs are in the high-impedance state. |
| An (n = 0 to 7) (input/output) | Eight bidirectional lines carry the A register inputs or B register outputs |
| Bn (n = 0 to 7) (input/output) | Eight bidirectional lines carry the B register inputs or A register outputs |

FIGURE 1. Terminal connections.

| A or B register functional table | | | | |
|---|---|---|---|---|
| Inputs | | | Internal | Function |
| Data | CP | $\overline{CE}$ | Q | |
| X | X | H | NC | Hold data |
| L | ↑ | L | L | Load data |
| H | ↑ | L | H | |

| Output control table | | | |
|---|---|---|---|
| $\overline{OE}$ | Internal Q | Outputs | Function |
| H | X | Z | Disable outputs |
| L | L | L | Enable outputs |
| L | H | H | |

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance
NC = No change
↑ = Low-to-high transition

FIGURE 2. Truth tables.

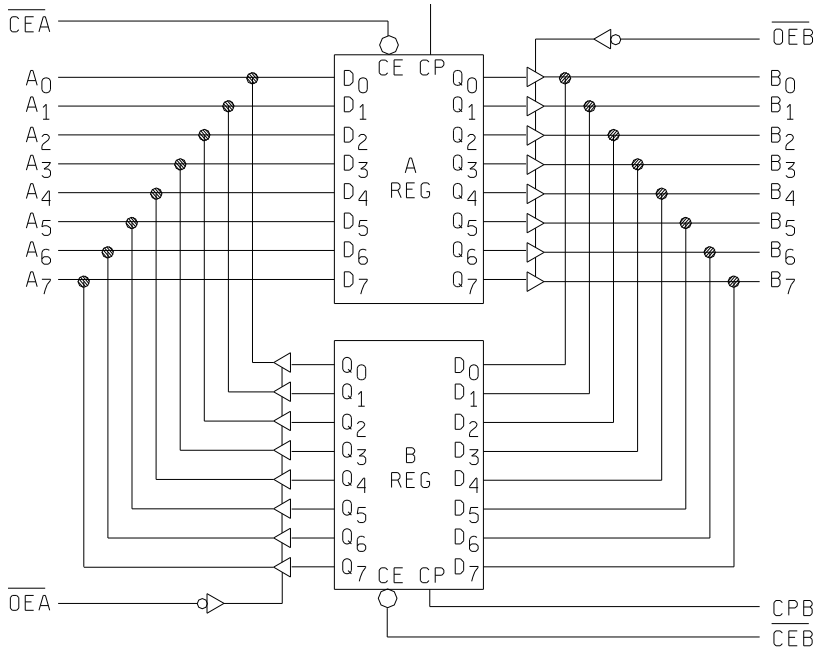
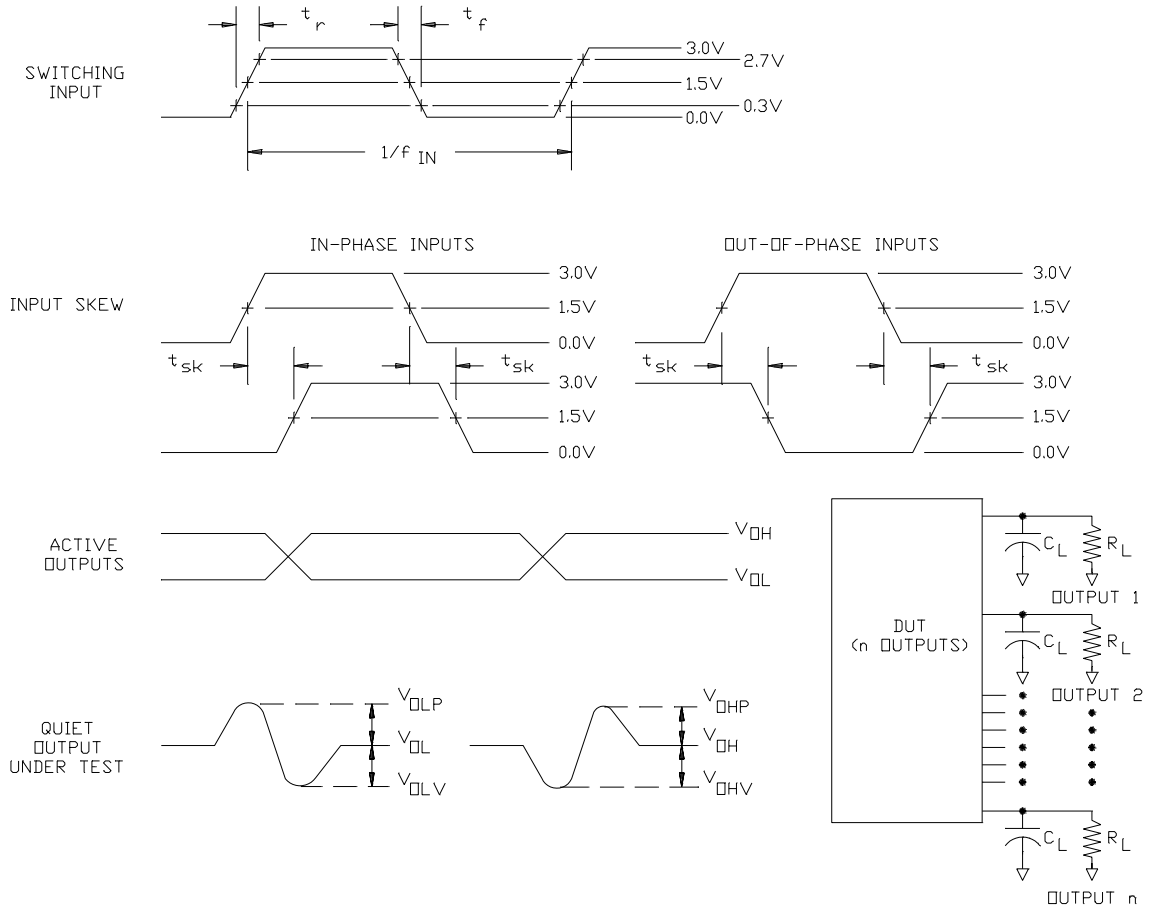



FIGURE 3. Logic diagram




NOTES:

1. $C_L$ includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. $R_L$ = 450Ω ±1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
   a. $V_{IN}$ = 0.0 V to 3.0 V; duty cycle = 50 percent; $f_{IN} \geq$ 1 MHz.
   b. $t_r$, $t_f$ = 3 ns ±1.0 ns. For input signal generators incapable of maintaining these values of $t_r$ and $t_f$, the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 3.0 ns ±1.0 ns; skew between any two switching inputs signals ($t_{sk}$): ≤ 250 ps.

FIGURE 4. Ground bounce load circuit and waveforms.

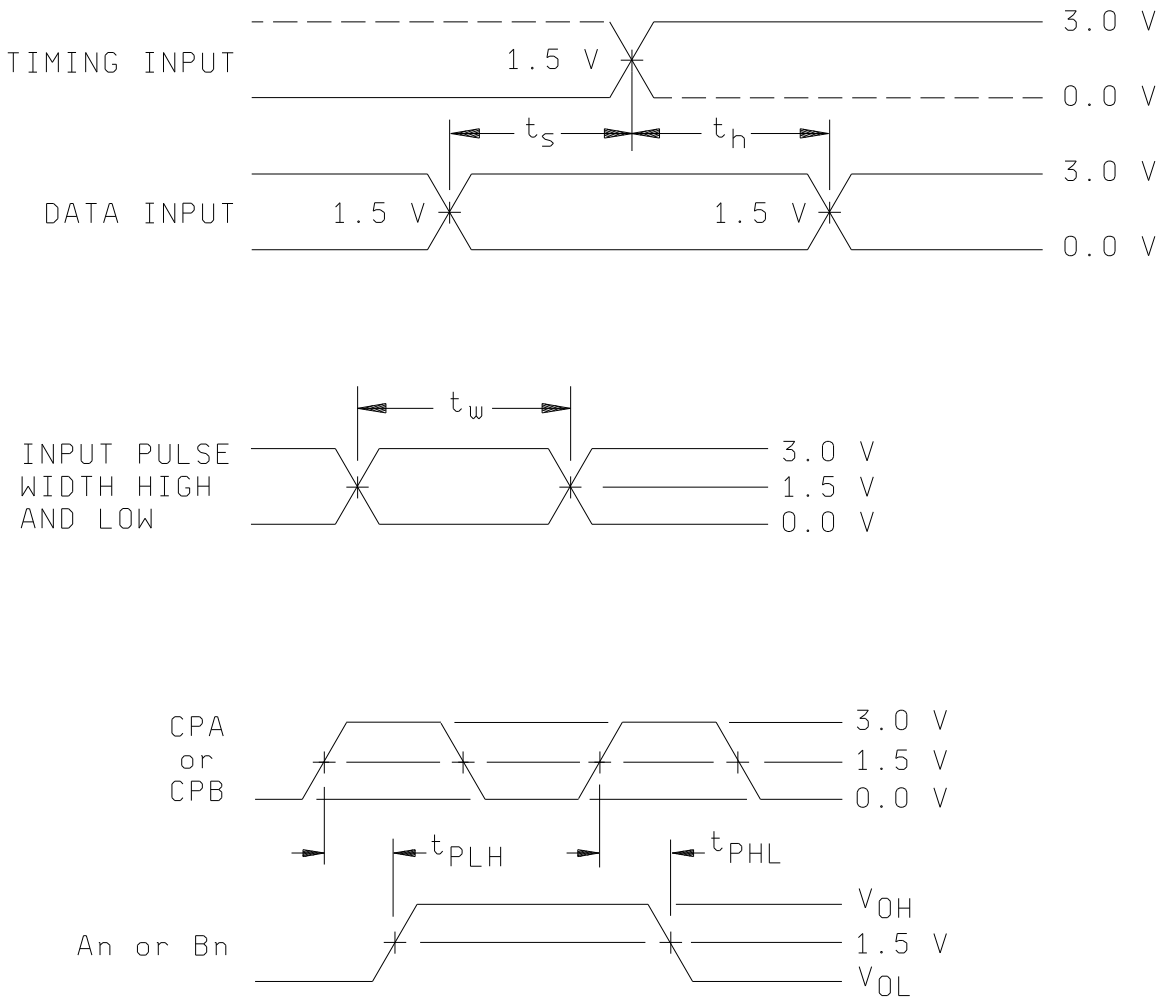
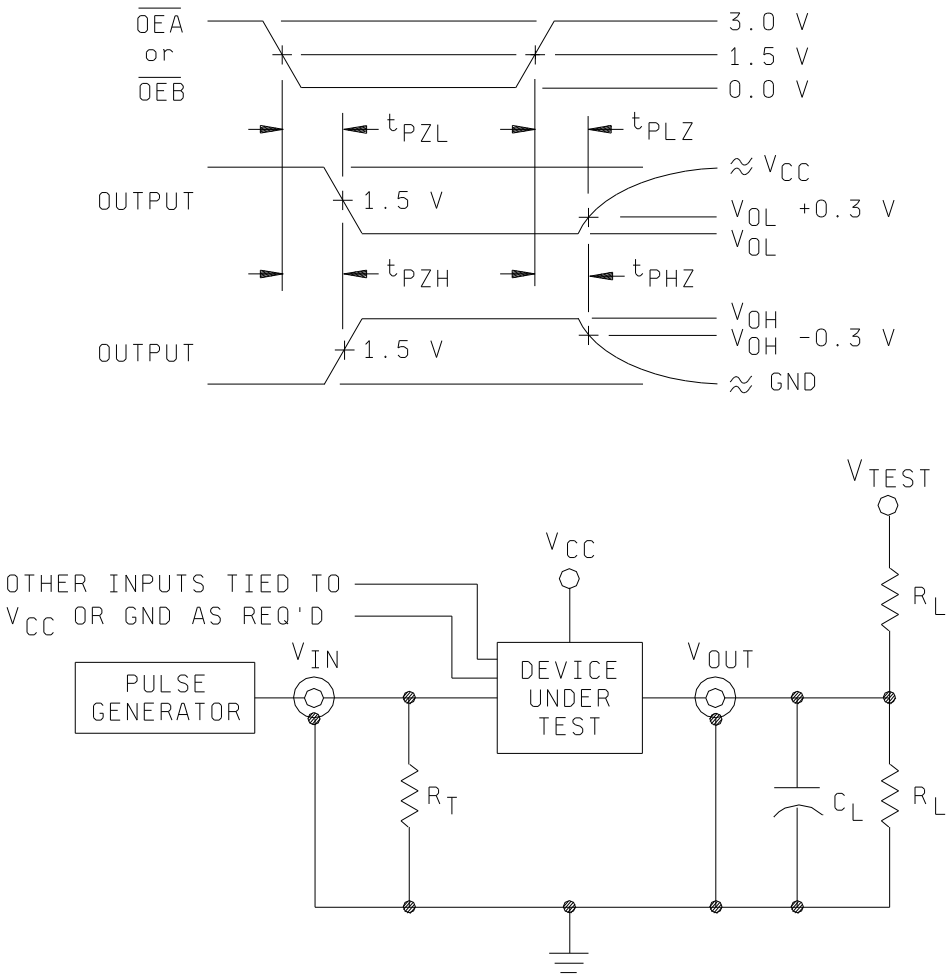



FIGURE 5. Switching waveforms and test circuit.




NOTES:

1. When measuring $t_{PLZ}$ and $t_{PZL}$: $V_{TEST}$ = 7.0 V.
2. When measuring $t_{PHZ}$, $t_{PZH}$, $t_{PLH}$ and $t_{PHL}$: $V_{TEST}$ = open.
3. The $t_{PZL}$ and $t_{PLZ}$ reference waveform is for the output under test with internal conditions such that the output is at $V_{OL}$ except when disabled by the output enable control. The $t_{PZH}$ and $t_{PHZ}$ reference waveform is for the output under test with internal conditions such that the output is at $V_{OH}$ except when disabled by the output enable control.
4. $C_L$ = 50 pF minimum or equivalent (includes test jig and probe capacitance).
5. $R_L$ = 500Ω or equivalent.
6. $R_T$ = 50Ω or equivalent.
7. Input signal from pulse generator: $V_{IN}$ = 0.0 V to 3.0 V; PRR ≤ 10 MHz; $t_r$ ≤ 2.5 ns; $t_f$ ≤ 2.5 ns; $t_r$ and $t_f$ shall be measured from 0.3 to 2.7 V and 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
8. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
9. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit - Continued.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. $C_{IN}$ and $C_{I/O}$ shall be measured only for initial qualification and after process or design changes which may affect capacitance. $C_{IN}$ and $C_{I/O}$ shall be measured between the designated terminal and GND at a frequency of 1 MHz. For $C_{IN}$ and $C_{I/O}$, test all applicable pins on five devices with zero failures.

For $C_{IN}$ and $C_{I/O}$, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the $C_{IN}$ and $C_{I/O}$ tests. The device manufacturer may then test one device functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table I, herein. The device manufacturer shall submit to DESC-EC the device functions listed in each functional group and the test results for each device tested.

c. Ground and $V_{CC}$ bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. $V_{OLP}$, $V_{OLV}$, $V_{OHP}$, and $V_{OHV}$ shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The package type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DESC-EC data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each $V_{OLP}$, $V_{OLV}$, $V_{OHP}$, and $V_{OHV}$ from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DESC-EC of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DESC-EC data from testing on both fixtures that shall include all measured peak values for each device tested and detailed oscilloscope plots for each $V_{OLP}$, $V_{OLV}$, $V_{OHP}$, and $V_{OHV}$ from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

For $V_{OHP}$, $V_{OHV}$, $V_{OLP}$, and $V_{OLV}$, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same test values when tested in accordance with table I, herein. The device manufacturer shall set a functional group limit for the $V_{OHP}$, $V_{OHV}$, $V_{OLP}$, and $V_{OLV}$ tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I, herein. The device manufacturer shall submit to DESC-EC the device functions listed in each functional group and test results, along with the oscilloscope plots, for each device tested.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth tables in figure 2 herein. The test vectors used to verify the truth tables shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth tables in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. $T_A$ = +125° C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

| Test requirements | Subgroup (in accordance with MIL-STD-883, TM 5005, table I) | Subgroups (in accordance with MIL-I-38535, table III ) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | - - - | 1 | 1 |
| Final electrical parameters (see 4.2) | 1/ 1, 2, 3, 4, 5, 6, 7 8, 9, 10, 11 | 1/ 1, 2, 3, 4, 5, 6 7, 8, 9, 10, 11 | 2/ 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 |
| Group A test requirements (see4.4) | 1, 2, 3, 4, 5, 6, 7 8, 9, 10, 11 | 1, 2, 3, 4, 5, 6, 7 8, 9, 10, 11 | 1, 2, 3, 4, 5, 6, 7 8, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 1, 2, 3, 4, 5, 6 | 1, 2, 3, 4, 5, 6 | 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 |
| GroupD end-point electrical parameters (see 4.4) | 1,2, 3 | 1,2, 3 | 1,2, 3 |
| Group E end-point electrical parameters (see 4.4) | 1, 4, 7, 9 | 1, 4, 7, 9 | 1, 4, 7, 9 |

1/ PDA applies to subgroups 1 and 4 (i.e., $I_{CCT}$ only).
2/ PDA applies to subgroups 1, 4, and 7.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331, and as follows:

| | |
|---|---|
| GND | Ground zero voltage potential. |
| $I_{CC}$ | Quiescent supply current. |
| $I_{IL}$ | Input current low. |
| $I_{IH}$ | Input current high. |
| $T_C$ | Case temperature. |
| $T_A$ | Ambient temperature. |
| $V_{CC}$ | Positive supply voltage. |
| $C_{IN}$ | Input terminal-to-GND capacitance. |
| $V_{IC-}$ | Negative input clamp voltage. |

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

| Military documentation format | Example PIN under new system | Manufacturing source listing | Document listing |
|---|---|---|---|
| New MIL-H-38534 Standardized Military Drawings | 5962-XXXXXZZ(H or K)YY | QML-38534 | MIL-BUL-103 |
| New MIL-I-38535 Standardized Military Drawings | 5962-XXXXXZZ(Q or V)YY | QML-38535 | MIL-BUL-103 |
| New 1.2.1 of MIL-STD-883 Standardized Military Drawings | 5962-XXXXXZZ(M)YY | MIL-BUL-103 | MIL-BUL-103 |

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 94-06-23

Appoved sopurces of supply for SMD 5962-92204 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agree to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

| Standarddized military drawing PIN | Vendor CAGE number | Vendor similar PIN 1/ |
|---|---|---|
| 5962-9220401MKX | 61772 | IDT29FCT52ATEB |
| 5962-9220401MLX | 61772 | IDT29FCT52ATDB |
| 5962-9220401M3X | 61772 | IDT29FCT52ATLB |
| 5962-9220402MKX | 61772 | IDT29FCT52BTEB |
| 5962-9220402MLX | 61772 | IDT29FCT52BTDB |
| 5962-9220402M3X | 61772 | IDT29FCT52BTLB |
| 5962-9220403MKX | 61772 | IDT29FCT52CTEB |
| 5962-9220403MLX | 61772 | IDT29FCT52CTDB |
| 5962-9220403M3X | 61772 | IDT29FCT52CTLB |

1/ Caution. Do not use this number for item acquisition. Items accquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 61772 | Integrated Devices Technology Inc.<br>3236 Scott Boulevard<br>P.O. Box 58015<br>Santa Clara, CA 95052 |